Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-8 (Canceled)

Claim 9 (Currently Amended): A method for manufacturing a semiconductor device, comprising:

~~a first step of~~ forming on a substrate a plurality of gate electrodes having offset nitride films and gate insulation films;

~~a second step of~~ forming a silicon oxide layer ~~including a silicon oxide film~~ so as to cover said substrate and said gate electrodes;

~~a third step of~~ forming a lower side wall spacer precursor layer that is thinner than said gate electrodes by etching said silicon oxide layer;

~~a fourth step of~~ forming a silicon nitride layer ~~including a silicon nitride film~~ so as to cover said lower side wall spacer precursor layer;

~~a fifth step of~~ successively etching said silicon nitride layer and said lower side wall spacer precursor layer so as to form ~~and thereby forming~~ side wall spacers having a structure consisting of [[an]] upper side wall spacer ~~in which a~~ portions and lower side

wall spacer portions, said upper side wall spacer portions being formed of said silicon nitride layer remaining ~~film remains~~ on [[the]] upper side walls of said gate electrodes ~~of the side wall~~, and [[a]] said lower side wall spacer portions being formed of said ~~in which a~~ silicon oxide layer remaining ~~film remains~~ on [[the]] lower side walls of said gate electrodes ~~of the side wall~~;

~~a sixth step of~~ forming an interlayer insulation film so as to cover said gate electrodes having said [[where]] side wall spacers ~~have been~~ formed thereon; and

~~a seventh step of~~ etching said [[the]] interlayer insulation film ~~and thereby self-aligningly forming~~ to form self-aligned contact holes that go through said interlayer insulation film,

wherein said forming a plurality of gate electrodes comprises forming said gate electrodes so as to provide a dense region where said gate electrodes are densely gathered and a sparse region where said gate electrodes are more scattered, so that a film thickness of said silicon oxide layer in said dense region is greater than a film thickness of said silicon oxide layer in said sparse region,

the method further comprising performing chemical mechanical polishing to smooth out said silicon oxide layer over a wide area, prior to said forming a lower side wall spacer precursor layer.

Claim 10 (Canceled)

Claim 11 (Currently Amended): A method for manufacturing a semiconductor device according to Claim 9,

~~wherein, in said first step, a plurality of said gate electrodes are formed so as to constitute a dense region where said gate electrodes are densely gathered and a sparse region where said gate electrodes are more scattered~~[[,]]

wherein during ~~the formation of~~ said forming a silicon oxide layer ~~in said second step~~, ~~the film~~ layer formation ~~material or film formation~~ conditions [[is or]] are set so that ~~the space~~ spaces between said gate electrodes in said dense and sparse regions are ~~region will be~~ filled in by said silicon oxide layer ~~and the film thickness on said upper side of said gate electrodes in said sparse region will be greater than the film thickness at said gate electrode side walls of said sparse region~~, and

~~in the third step~~[[,]] wherein said forming a lower side wall spacer precursor layer ~~is formed by~~ comprises etching said silicon oxide layer so that [[the]] film thickness of said silicon oxide layer between [[at]] said gate ~~electrode side walls of~~ electrodes in said dense region is ~~greater than the~~ equal to film thickness of said silicon oxide layer between [[at]] said gate electrodes in ~~electrode side walls of~~ said sparse region.

Claim 12 (Currently Amended): A method for manufacturing a semiconductor device according to Claim 11,

wherein said silicon oxide layer is formed using PSG (phosphosilicate glass),

BPSG (boron-phosphosilicate glass), P-TEOS · NSG (non-doped silicate glass by plasma CVD using tetraethylorthosilicate), or P-SiH_4 · NSG (non-doped silicate glass by plasma CVD using tetraethylorthosilicate).

Claims 13-14 (Canceled)

Claim 15 (New): A method for manufacturing a semiconductor device, comprising:

forming first and second gate electrodes on a substrate, wherein the first gate electrodes are formed in a first region with a first density, and the second gate electrodes are formed in a second region with a second density, the second density being lower than the first density;

forming a silicon oxide layer so as to cover the substrate and the first and second gate electrodes, a film thickness of said silicon oxide layer in the first region is greater than a film thickness of said silicon oxide layer in the second region;

performing chemical mechanical polishing to smooth out said silicon oxide layer;

forming a lower side wall spacer precursor layer that is thinner than the first and second gate electrodes by etching said silicon oxide layer, after said performing chemical mechanical polishing;

forming a silicon nitride layer so as to cover the lower side wall spacer precursor layer;

successively etching the silicon nitride layer and the lower side wall spacer precursor layer so as to form side wall spacers having a structure consisting of first and second upper side wall spacer portions and first and second lower side wall spacer portions, the first upper side wall spacer portions being formed of said silicon nitride layer on upper side walls of the first gate electrodes, the first lower side wall spacer portions being formed of said silicon oxide layer on lower side walls of the first gate electrodes, the second upper side wall spacer portions being formed of said silicon nitride layer on upper side walls of the second gate electrodes, and the second lower side wall spacer portions being formed of said silicon oxide layer on lower side walls of the second gate electrodes;

forming an interlayer insulation film so as to cover the gate electrodes having the side wall spacer portions formed thereon; and

etching the interlayer insulation film to thereby form self-aligned contact holes that go through said interlayer insulation film.

Claim 16 (New): A method for manufacturing a semiconductor device according to claim 15, wherein the silicon oxide layer is formed using phosphosilicate glass, boron-phosphosilicate glass, P-TEOS · non-doped silicate glass formed by plasma deposition using tetraethylorthosilicate glass, or P-SiH_4 · non-doped silicate glass formed by plasma deposition using tetraethylorthosilicate glass.

Claim 17 (New): A method for manufacturing a semiconductor device according to Claim 15, wherein during said forming a silicon oxide layer, layer formation conditions are set so that spaces between the first gate electrodes in the first region and spaces between the second gate electrodes in the second region are filled in by said silicon oxide layer, and

wherein said forming a lower side wall spacer precursor layer comprises etching said silicon oxide layer so that film thickness of said silicon oxide layer between the first gate electrodes is equal to film thickness of said silicon oxide layer between the second gate electrodes.